



UNITED STATES PATENT AND TRADEMARK OFFICE

Am

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,899	06/29/2000	Alain Benayoun	FR9-1999-0027-US1	7629

7590 11/10/2003

John R. Pivnichny, IBM Corporation
Intellectual Property Law, Dept. IQOA/Bldg. 040-3
1701 North Street
Endicott, NY 13760

EXAMINER

LIN, KENNY S

ART UNIT	PAPER NUMBER
----------	--------------

2154

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/606,899

Applicant(s)

BENAYOUN ET AL.

Examiner

Kenny Lin

Art Unit

2154

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-10 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- a. The following term lack proper antecedence basis:

- i. Interconnection logic block – claim 10 (The term is inconsistent with “Interconnection logic means” introduced in claim 1).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Papadopoulos et al (hereinafter Papadopoulos), US 5,430,850.

Art Unit: 2154

6. As per claim 1, Papadopoulos taught the invention as claimed including a hardware device for concurrently processing a plurality of tasks associated with an algorithm which includes a number of processes some of which are dependant on binary decisions (abstract, col.4, lines 67-68, col.5, lines 1-5) said device comprising:

- a. A plurality of task units for processing data, making decisions and/or processing data and making decisions (col.5, lines 10-17);
- b. A task interconnection logic means interconnecting the task units for communicating actions from a source task unit to a destination task unit (col.4, lines 64-66, col.5, lines 40-45, col.20, lines 8-23).
- c. Each of said task units including a processor for executing the steps of the associated task in response to a received request action (col.5, lines 10-17); and,
- d. A status manger for handling actions from source task units and building actions to be sent to destination task units (col.26, lines 54-60).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papadopoulos, US 5,430,850.

Art Unit: 2154

9. As per claim 2, Papadopoulos taught the invention substantially as claimed in claim 1. Papadopoulos further taught that wherein said actions communicated from a source task unit to a destination task unit are START used to activate the processor of said destination task unit (col.4, lines 46-58, col.5, lines 17-23). Papadopoulos did not specifically teach the actions to include KILL used to cancel the task associated with said destination task unit and VALID used to confirm that task associated with said destination task unit corresponds to a decision included in said task. However, it would have been obvious to add different commands to perform desired actions according to administering needs. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Papadopoulos's system with commands such as KILL and VALID to perform administrative actions.

10. As per claim 3, Papadopoulos taught the invention substantially as claimed in claim 2. Papadopoulos further taught that wherein said status manager activates said processor for processing the steps of the task associated with said destination task unit when the action received from a source task unit is START (col.4, lines 46-58, col.5, lines 17-23).

11. As per claim 4, Papadopoulos taught the invention substantially as claimed in claim 3. Papadopoulos further taught that wherein said status manager is a state machine (col.26, lines 54-60).

Art Unit: 2154

12. As per claim 5, Papadopoulos taught the invention substantially as claimed in claim 3. Papadopoulos further taught that wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow (col.5, lines 24-39). Papadopoulos did not specifically teach that each one of said control/data registers comprising a control field composed of a completion bit set to 1 when the associated task is completed, a validation bit set to 1 when the associated task is validated and a L/R bit indicating that the output in the algorithm flow is left or right when said task includes a decision. However, it would have been obvious to use bits in data register to indicate the condition of the associated task. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use specific bit(s) to indicate the status of the task in Papadopoulos' system according to design choice.

13. As per claim 6, Papadopoulos taught the invention substantially as claimed in claim 5. Papadopoulos did not specifically teach that wherein each of said control/data registers includes a data field which is loaded if necessary by said status manager activated by an action received from a source task unit, said processor using these data for executing the task associated with said task unit and replacing them if necessary. However, it would have been obvious to load a data field or execute any job when an action is received. It would have been obvious to one of ordinary skill in the art at the time the invention was made to load a data field by the status manager in Papadopoulos's system when the status manager receives an action commanding to do so.

14. As per claim 7, Papadopoulos taught the invention substantially as claimed in claim 6. Papadopoulos did not specifically teach that wherein said completion bit is sent by said processor to said status manager after completion of the task execution. However, it is obvious to send notifications to notify the status manager of the current status. It would have been obvious to one of ordinary skill in the art at the time the invention was made to send a completion bit to the status manager in Papadopoulos' system to notify the completion of task execution in the system.

15. As per claim 8, Papadopoulos taught the invention substantially as claimed in claims 5-7. Papadopoulos did not specifically teach that wherein said control/data register corresponding to a specific instance is cleared by said status manager when this one receives an action KILL for the task associated with said task unit and for said specific instance. However, it would have been obvious that the objective of a KILL/Delete action is to remove a specific instance. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a KILL action in Papadopoulos's system to clear a specific instance.

16. As per claim 9, Papadopoulos taught the invention substantially as claimed in claims 5-7. Papadopoulos did not specifically teach that wherein each of said task units further comprises two configuration registers CONFIG.L and CONFIG.R which are respectively selected by the binary value of said bit L/R of the control/data register of the instance being considered, the contents of said configuration registers being loaded at the beginning of the algorithm processing for defining the task to be activated, the action to be performed and the instance to be considered. However, the use of CONFIG.L and CONFIG.R registers is well known and would have been

obvious to use them to define the tasks that need to be activated. It would have been obvious to use CONFIG.L and CONFIG.R in Papadopoulos' system as the configuration registers to define the tasks, actions and instances.

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Papadopoulos as applied to claims 1-9 above, and further in view of Fairfield et al (hereinafter Fairfield), US 5,321,842.

18. As per claim 10, Papadopoulos taught the invention substantially as claimed in claims 1-7. Papadopoulos did not specifically teach that wherein said task interconnection logic means is composed of three-state drivers each one of said drivers being associated with one of said tasks as input task and a number of buses equal to the number of said tasks as output tasks, one of said buses being selected by the driver corresponding to an input task after decoding an action word by said driver. However, the use of three-state driver is well known in the art and would have been obvious to implement the task interconnection logic means with three-state drivers.

Fairfield taught a processor using three-state drivers (col.2, lines 4-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Papadopoulos and Fairfield because Fairfield's teaching of using three-state drivers help to employ feedback to the processor in Papadopoulos' system.

Conclusion

Art Unit: 2154

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Podlesny et al, US 6,320,446.

Huppenthal et al, US 6,247,110.

Culbert, US 5,838,968.

Broder et al, US 5,991,808.

Neches et al, US 4,412,285.

Green et al, US 6,496,881.

20. A shortened statutory period for reply to this Office action is set to expire THREE MONTHS from the mailing date of this action.


21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenny Lin whose telephone number is (703)305-0438. The examiner can normally be reached on 8 AM to 5 PM Tuesday to Friday and every other Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703)305-9678. Additionally, the fax numbers for Group 2100 are as follows:

Official Responses: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-6121.

ksl
November 3, 2003


ZARNI MAUNG
PRIMARY EXAMINER